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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,955	12/14/2001	Harry Chuang	TS01-1372	7559

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/017,955	Applicant(s) CHUANG, HARRY	
	Examiner Thanhha Pham	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 1-46 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

- "depositing a first layer of semiconductor material over the surface of said substrate including the surface of said at least one point of electrical contact having been provided over the surface of said substrate; patterning and etching said first layer of semiconductor material, creating at least one first opening through said first layer of semiconductor material that aligns with at least one point of electrical contact having provided over the surface of said substrate; creating at least one first conductive via in said at least one first opening created through said first layer of semiconductor material; depositing a first layer of conductive material over the surface of said first layer of semiconductor material, including the surface of said at least one first conductive via created in said at least one first opening created through said first layer of semiconductor material; and patterning and etching said first layer of conductive material, creating at least

one first wide-line of interconnect metal over the surface of said first layer of semiconductor material overlying at least one first conductive via created in said at least one first opening created through said first layer of semiconductor material, said at least one first conductive via and said at least one first wide-line of interconnection metal making contact in a first interface area, additionally creating at least one first slot through said first layer of conductive material being separated from said first interface by a measurable distance" is not supported by specification and figures.

- "depositing a second layer of semiconductor material over the surface of said first layer of semiconductor material, including the surface of said at least one first wide-line of interconnect metal created over the surface of said first layer of semiconductor material; patterning and etching said second layer of semiconductor material, creating at least one second opening through said second layer of semiconductor material that aligns with at least one first wide-line interconnect metal created over the surface over the surface of said first layer of semiconductor material; creating at least one second conductive via in said at least one second opening created through said second layer of semiconductor material; depositing a second layer of conductive material over the surface of said second layer of semiconductor material, including the surface of said at least one second conductive via created in said at least one second opening created through said second layer of semiconductor material; and patterning and etching said second layer of conductive material, creating at least one second wide-line

of interconnect metal over the surface of said second layer of semiconductor material overlying at least one second conductive via created in said at least one second opening created through said second layer of semiconductor material, said at least one second conductive via and said at least one second wide-line of interconnection metal making contact in a second interface area, additionally creating at least one second slot through said second layer of conductive material being separated from said second interface by a measurable distance" is not supported by specification and figures.

- "semiconductor material comprising a dielectric material" is not supported by specification or figures.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1,

Lines 22-25, it is not clear what overlying said at least one first conductive via -- said at least one first wide-line of interconnect metal OR the surface of said first layer of semiconductor material?

Line 28-30, it is not clear what additionally creating at least one first slot

With respect to claim 2,

"a first, second and third surface area or combination thereof" is redundant – when said at least one first slot comprises a first, a second and a third surface area, it also means that said at least one first slot comprises a combination of first, second, and third surface areas.

in addition, it is not clear "a measurable distance" (s) cited in lines 2, 15-16, 18-19, and 21-22 are the same to each other or not.

With respect to claim 9,

It is not clear how a semiconductor material can comprise a dielectric material?

With respect to claim 13,

Lines 21-24, it is not clear what overlying said at least one second conductive via -- said at least one second wide-line of interconnect metal OR the surface of said second layer of semiconductor material?

Line 27-29, it is not clear what additionally creating at least one second slot

With respect to claim 14,

"a first, second and third surface area or combination thereof" is redundant – when said at least one second slot comprises a first, a second and a third surface area, it also means that said at least one second slot comprises a combination of first, second, and third surface areas.

in addition, it is not clear "a measurable distance" (s) cited in lines 2, 15-16, 18-19, and 21-22 are the same to each other or not.

With respect to claim 21,

It is not clear how a semiconductor material can comprise a dielectric material?

With respect to claim 25,

Line 13, it is not clear what additionally creating at least one slot.

With respect to claim 26,

Lines 11-12, it is not clear if there is any relationship between "at least one conductive via" in claim 26 to "at least one interconnect via" in claim 25 or not

Line 18, it is not clear that "at least one wide-line of interconnect metal" as cited in claim 26 is the same to "at least one wide-line of interconnect metal" as cited in claim 25 or not.

lines 18-21, it is not clear what overlying said at least one conductive via -- said at least one wide-line of interconnect metal OR the surface of said layer of semiconductor material?

Line 24-26, it is not clear what additionally creating at least one slot

With respect to claim 27,

"a first, second and third surface area or combination thereof" is redundant – when said at least one slot comprises a first, a second and a third surface area, it also means that said at least one slot comprises a combination of first, second, and third surface areas.

in addition, it is not clear "a measurable distance" (s) cited in lines 2, 15, 17, and 19 are the same to each other or not.

With respect to claim 34,

It is not clear how a semiconductor material can comprise a dielectric material?

With respect to claims 38-46,

It is not clear that "a measurable distance" cited in each of claims 38-46 are the same to each other or not? Do they have the same value of "measurable distance"?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 and 25-27, and 38-46, as being best understood are rejected under 35 U.S.C. 102(b) as being anticipated by Tetsuo Uchiyama [JP 04-007835].

Tetsuo Uchiyama discloses the claimed method of creating interconnect metal comprising steps of:

providing a substrate (1), at least one point of electrical contact (2) having been provided over the surface of said substrate;

creating at least one layer of interconnect metal (5) over the surface of substrate, said at least one layer of interconnect metal comprising at least one interconnect via (interconnect metal 5 in the via 4) in addition to comprising at least one wide-line of interconnect metal, said at least one interconnect via overlying said at least one point of electrical contact having been provided over the surface of said substrate, said at least

one wide-line of interconnect metal overlying said at least one interconnect via, said at least one interconnect via and said at least one wide-line of interconnect metal making contact in a interface area; and

additional creating at least one slot (6) through said at least one wide-line of interconnect metal being separated from said interface area by a measurable distance;

wherein said creating at least one layer of interconnect metal over the surface of said substrate comprising:

depositing a passivation layer (3) over the surface of said substrate including the surface of said at least one point of electrical contact having been provided over the surface of said substrate;

patterning and etching passivation layer, creating at least one opening (4) through said passivation layer that aligns with at least one point of electrical contact having provided over the surface of said substrate;

creating said at least one interconnect via in said at least one opening created through said passivation layer;

depositing a layer of conductive material over the surface of said passivation layer, including the surface of said at least one interconnect via created in said at least one opening created through said first layer of semiconductor material; and

patterning and etching said layer of conductive material, creating said at least one wide-line of interconnect metal over the surface of passivation layer; said at least one wide-line of interconnect metal overlying at least one

interconnect via created in said at least one opening created through passivation layer, said at least one first interconnect via and said at least one wide-line of interconnect metal making contact in said interface area, said patterning and etching additionally creating said at least one slot through said first layer of conductive material being separated from said interface by said measurable distance.

With respect to claims 2 and 27, Tetsuo Uchiyama teaches said at least one slot comprising a first surface area (a left slit 6, see notation in figure 2 for details), a second surface area (front portion of the right slit 6, see notation in figure 2 for details) and a third surface area (back portion of the right slit 6, see notation in figure 2 for details); said first surface area, said second surface area and said third surface area being a rectangle or a square; a side of said first surface area being parallel with a first side of said at least one interconnect via; a side of said second surface area being parallel with a second side of said at least one interconnect via; a side of said third surface area being parallel with a third side of said at least one interconnect via; a side of said first surface area being separated from a first side of said at least one interconnect via; a side of said second surface area being separated from a second side of said at least one interconnect via; a side of said third surface area being separated from a third side of said at least one interconnect via.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-37, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricocos et al [US 6,090,710] in view of Kazushiko Kasahara [JP 03-200332].

Andricocos et al, figs 1-11 and col 1-8, discloses a method of creating interconnect metal comprising steps of:

providing a substrate, at least one point of electrical contact having been provided over the surface of said substrate (see fig 7);

depositing a first insulator layer over the surface of said substrate including the surface of said at least one point of electrical contact having been provided over the surface of said substrate;

patterning and etching said first insulator layer, creating at least one first opening through said first insulator layer that aligns with at least one point of electrical contact having provided over the surface of said substrate;

creating at least one first conductive via (comprising Cu) in said at least one first opening created through said first insulator layer;

depositing a first layer of conductive material (comprise Cu) over the surface of said first insulator layer, including the surface of said at least one first conductive via created in said at least one first opening created through said first insulator layer;

patterning and etching said first layer of conductive material, creating at least one first wide-line of interconnect metal over the surface of said first insulator layer, said at least one first wide-line of interconnect metal overlying at least one first conductive via created in said at least one first opening created through said first insulator layer, said at least one first conductive via and said at least one first wide-line of interconnection metal making contact in a first interface area;

depositing a second insulator layer over the surface of said first insulator layer, including the surface of said at least one first wide-line of interconnect metal created over the surface of said first insulator layer;

patterning and etching said second insulator layer, creating at least one second opening through said second insulator layer that aligns with at least one first wide-line interconnect metal created over the surface of said first insulator;

creating at least one second conductive via (comprising Cu) in said at least one second opening created through said second insulator;

depositing a second layer of conductive material (comprising Cu) over the surface of said second insulator layer, including the surface of said at least one second conductive via created in said at least one second opening created through said second insulator layer; and

patterning and etching said second layer of conductive material, creating at least one second wide-line of interconnect metal over the surface of said second insulator layer overlying at least one second conductive via created in said at least one second opening created through said second insulator layer, said at least one second conductive via and said at least one second wide-line of interconnection metal making contact in a second interface area.

Andricacos et al does not teach creating first and second slots respectively through said first and second layers of conductive material wherein said first and second slots being respectively separated from said first and second interfaces areas, each of first and second slots comprising a first surface area, a second surface area and a third surface area wherein said first, second and third surface areas being a rectangle or square, sides of said first, second and third surface areas repectively being separated and parallel to first, second and third side of first or second conductive via.

Kazuhiko Kasahara teaches creating slot (16, fig 2) comprising first, second and third surface areas in a wide-line of interconnect metal (14) to reduce stress in the wide-line of interconnect metal (14) for improve a interconnection operation. Kazuhiko Kashara also teaches said first, second and third surfaces areas (being a rectangle or a square) respectively separated and parallel to first, second and third side of a conductive via (15).

It would have been obvious for those skilled in the art to combine the teaching of Kazuhiko Kasahara to the process of Andricacos et al to create the first and second

slots as being claimed in the wide-lines of interconnect metal for reducing stress to improve interconnection ability in a device.

With respect to claims 3-8, 12, 15-20, 24, 28-33, and 37, dimensions of first, second and third surface areas, distances between the first, second or third surface areas to the conductive via, widths of the wide-lines of interconnect metal are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> In re Aller 105 USPQ233, 255 (CCPA). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

5. Claims 38-46, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al in view of Kazuhiko Kasahara as applied to claims 2, 14 or 27 above, in futher view of Lur et al [US 5,924,006].

Andricocos et al in view of Kazuhiko Kasahara substantially discloses the claimed method except teaching that the sides of first, second and third surface areas can be overlying on each other over measurable distances.

However, creating the slot with such overlapping surface areas in wide-line interconnect metal for reducing stress is obvious for those skilled in the art as a matter design choice. See Lur et al as an evidence that teaches forming a slot (narrow trench surrounding a metal line to reduce stress) comprising overlapping first, second and third surface (to form continuous trench surrounding the metal line).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (703) 308-6172. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-3432 for regular communications and (703) 308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham
July 10, 2002

Tuan H. Nguyen
Primary Examiner